CLAIMS

What is claimed is:

1. Architecture that facilitates a reference voltage in a multi-bit memory (400), comprising:

a multi-bit memory core (401) including a plurality of data cells (200) for storing data;

first and second reference arrays (408, 410) of a plurality of multi-bit reference cells (182, 184), the first and second reference arrays (408, 410) fabricated on the memory core (401); and

a first bit value of a first reference cell (182) of the first reference array (408) averaged with a second bit value of a second reference cell (184) of the second reference array (410) to arrive at the reference voltage.

2. The architecture of claim 1, the core (401) further comprising a sector (416) of multi-bit data cells (180) organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells (180) in a row and with associated bitlines (BLn) attached to the multi-bit data cells in a column, the first and second reference cells (182, 184) forming a multi-bit reference pair (185) that is programmed and erased with the multi-bit data cells (180) during programming and erase cycles.

3. The architecture of claim 2, the multi-bit reference pair (185) is associated with a word in a wordline (WL0), the multi-bit reference pair (185) utilized during reading of bits of the word.

4. The architecture of claim 2, the multi-bit reference pair (185) is associated with multi-bit data cells (180) in a wordline (WL0), the multi-bit reference pair (185) utilized during reading of bits in the wordline (WL0).

5. The architecture of claim 2, further comprising a plurality of the multi-bit reference pairs (185) associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair (185) utilized during reading of bits in the corresponding wordline (WL0).

6. The architecture of claim 2, the multi-bit reference pair (185) is associated with multi-bit data cells (180) in the sector (416), the multi-bit reference pair (185) utilized during reading of bits in the sector (416).

7. The architecture of claim 1, the memory core (401) including a plurality of data sectors (404, 406) that are accessible by the first and second reference arrays (408, 410), the first and second reference arrays (408, 410) located centrally of the plurality of data sectors (404, 406).

8. An integrated circuit comprising the memory (400) of claim 1.

9. A computer comprising the memory (400) of claim 1.

10. An electronic device comprising the memory (400) of claim 1.

11. The architecture of claim 1, the first and second reference arrays (408, 410) including corresponding reference cells (182, 184) that are interweaved among the data cells (180).

12. The architecture of claim 1, the memory core (401) further comprising a plurality of data sectors (404, 406), such that each data sector (416) is associated with at least one of the first reference array (408) and the second reference array (410) of multi-bit reference cells (182, 184).

13. Architecture that facilitates a reference voltage in a multi-bit memory (400), comprising:

a multi-bit memory core (401) for storing data, the memory core (401) including two groups (404, 406) of data sectors (416);

first and second reference arrays (408, 410) of a plurality of multi-bit reference cells (182, 184), the first and second reference arrays (408, 410) fabricated on the memory core (401) interstitial to the groups (404, 406) of data sectors (416); and

a first bit value of a first reference cell (182) of the first reference array (408) and a second bit value of a second reference cell (184) of the second reference array (410) forming a reference pair (185) whose respective bit values are averaged to arrive at the reference voltage.

14. The architecture of claim 13, the groups (404, 406) of data sectors (416) read in an interleaved manner with a selected reference pair (185).

15. The architecture of claim 13, the first and second reference arrays (408, 410) precharged before being averaged.

16. The architecture of claim 13, further comprising a redundancy array (412) located at least one of proximate and adjacent to the groups (404, 406) of data sectors (416).

17. A method for providing a reference voltage in a multi-bit memory, comprising:

receiving a multi-bit memory core (401) for storing data;

providing first and second reference arrays (408, 410) of a plurality of multi-bit reference cells (182, 184), the first and second reference arrays (408, 410) fabricated on the memory core (401); and

averaging a first bit value of a first reference cell (182) of the first reference array (408) with a second bit value of a second reference cell (184) of the second reference array (410) to arrive at the reference voltage.

18. The method of claim 17, the core (401) further comprising a sector (416) of multi-bit data cells (180) organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells (180) in a row and with associated bitlines (BLn) attached to the multi-bit data cells (180) in a column, the first and second reference cells (182, 184) forming a multi-bit reference pair (185) that is programmed and erased with the multi-bit data cells (180) during programming and erase cycles.

19. The method of claim 18, the multi-bit reference pair (185) is associated with a word in a wordline (WL0), the multi-bit reference pair (185) utilized during reading of bits in the word.

20. The method of claim 18, the multi-bit reference pair (185) is associated with multi-bit data cells (180) in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the wordline (WL0).

21. The method of claim 18, further comprising a plurality of the multi-bit reference pairs (185) associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair (185) utilized during reading of bits in the corresponding wordline (WL0).

22. The method of claim 18, the multi-bit reference pair (185) is associated with multi-bit data cells (180) in the sector (416), the multi-bit reference pair (185) utilized during reading of bits in the sector (416).

23. The method of claim 17, the memory core (401) including a plurality of data sectors (404, 406) that are accessible by the first and second reference arrays (408, 410), the first and second reference arrays (408, 410) located centrally of the plurality of data sectors (404, 406).

24. A system for providing a reference voltage in a multi-bit memory, comprising:

means for providing a multi-bit memory core (401) for storing data;

means for providing first and second reference arrays (408, 410) of a plurality of multi-bit reference cells (180), the first and second reference arrays (408, 410) fabricated on the memory core (401); and

means for averaging a first bit value of a first reference cell (182) of the first reference array (408) with a second bit value of a second reference cell (184) of the second reference array (410) to arrive at the reference voltage.

25. The architecture of claim 24, the first and second reference arrays (408, 410) including corresponding reference cells (182, 184) that are interweaved among the data cells (180).

26. The architecture of claim 24, the memory core (401) further comprising a plurality of data sectors (404, 406), such that each data sector (416) is associated with at least one of the first reference array (408) and the second reference array (410) of multi-bit reference cells (182, 184).

27. The architecture of claim 24, further comprising a redundancy array (412) located at least one of proximate and adjacent to the groups (404, 406) of data sectors (416).